IN THE DESCRIPTION

Page 1, last paragraph, amend as follows:

US patent n° no. 5,999,355 describes an asynchronous receiver
such as the one mentioned in the opening paragraph. In accordance
with the cited patent, the equalizer is a tapped delay line (Finite
Impulse Response filter) with a tap spacing of Ts seconds. Control
of the equalizer is based on the classical LMS (Least Mean Square)
algorithm; that is to say, correlating the tap sequences with a
suitable error sequence produces updates of the equalizer tap
values. Classical LMS techniques normally apply to synchronous
receivers wherein error and tap sequences have the same sampling
rate and are phase synchronous. The asynchronous receiver described
in the cited patent thus comprises at least two provisions in order
that error and tap sequences have the same sampling rate and are
phase synchronous. The latter condition implies that any latency in
the error sequence should be matched by delaying the tap sequences
accordingly. The aforementioned two provisions include an inverse
sampling rate conversion (ISRC) for converting the synchronous
error sequence at the data rate 1/T into an equivalent error
sequence of sampling rate 1/Ts. The receiver, having an
asynchronously placed LMS-based adaptive equalizer, has two control
loops: a timing recovery loop or PLL (Phase locked loop) and an
equalizer's adaptation loop. Unless precautions are taken, the two
loops can interfere with each other, which may lead to instability.

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